REMARKS

Claims 1 and 7 are amended for the purpose of expediting prosecution. Claims 2 and 8 are canceled without prejudice.

New claims 19-24 are added to claim the invention in alternative language.

The Office Action does not establish that claims 1-3 and 6-9 are unpatentable under 35 USC §103(a) over US patent 6,096,091 to Hartman (hereinafter "Hartman") in view of US patent 6,247,110 to Huppenthal (hereinafter "Huppenthal"). The rejection is respectfully traversed because the Office Action does not establish a *prima facie* case of obviousness. However, independent claims 1 and 7 are amended for the purpose of expediting prosecution, the rejection is now moot. The claims are amended to make clear that design components are configured with parameters rather than implemented hardware components being configured with parameters.

This paper incorporates by reference all prior traversals of asserted correspondences of Hartman to the claim limitations. Furthermore, the alleged motivation for combining Huppenthal with Hartmann is conclusory, and it does not appear that the combination could be made with a reasonable likelihood of success.

The Office Action does not establish that claims 4 and 5 are unpatentable under 35 USC §103(a) over Hartman in view of Huppentahl and further in view of US patent 5,970,254 to Cooke et al. (hereinafter "Cooke"). The rejection is respectfully traversed because the Office Action does not establish a *prima facie* case of obviousness. The rejection is moot in view of the amendments made to the claims.

New claim 19 sets forth method for creating a design of a field programmable gate array-based (FPGA-based) system on chip (SoC). The method includes selecting hardware design components from a library in response to user input to a design tool executing on a processor; associating at least one parameter value with a first selected hardware design component in response to user input to the design tool; automatically associating by the design tool, without user specification of the association, the at least one parameter value with a second selected hardware design component; and generating by the design tool hardware description language (HDL) code from the first and second hardware design components using the at least one parameter value.

Claim 19 as a whole is not thought to be taught by the prior art of record. For example, there is no apparent teaching of in the prior art of record of selecting hardware design components from a library in response to user input to a design tool executing on a processor. Nor is there apparent teaching of associating at least one parameter value with a first selected hardware design component in response to user input to the design tool. Furthermore, the prior art of record is not thought to teach or suggest automatically associating by the design tool, without user specification of the association, the at least one parameter value with a second selected hardware design component. Finally, the prior art of record does not appear to teach the claimed generating of HDL code.

As to claims 20-22 depending from claim 19 should be allowable for at least the same reasons claim 19 is allowable.

Claims 23 and 24 are apparatus and system claims, respectively. Claims 23 and 24 are thought to be patentable over the prior art of record because these claims include functional limitations similar to those of claim 19, and claim 19 is thought to be patentable over the prior art of record.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 9, 2004.

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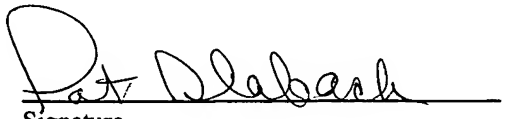
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